CLAIMS

What is claimed is:

1. A method for fabricating accurately located etched features on a semiconductor substrate, comprising the steps of:

   a) providing a semiconductor substrate with a top surface and a dielectric layer on the top surface;
   b) forming a patterned metal layer on the dielectric layer, wherein the patterned metal layer has a metal edge;
   c) forming a patterned resist layer on the dielectric layer and patterned metal layer, wherein the resist layer has a resist edge that is located on top of the metal layer such that the dielectric layer has an exposed area defined by the metal edge;
   d) etching away the dielectric layer from the exposed area;
   e) etching the semiconductor substrate where the dielectric layer is etched away in step (d).

2. The method of claim 1 wherein the semiconductor substrate is made of a material selected from the group consisting of silicon, doped silicon, and GaAs.

3. The method of claim 1 wherein the dielectric layer is made of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

4. The method of claim 1 wherein the patterned metal layer comprises a metal selected from the group consisting of chromium, nickel, titanium, platinum, aluminum, silver, copper and tantalum.

5. The method of claim 1 wherein step (d) comprises directional dry etching.

6. The method of claim 1 wherein step (d) comprises wet etching.

7. The method of claim 1 wherein step (e) comprises wet anisotropic etching.

8. The method of claim 1 wherein step (e) comprises directional dry etching.

9. The method of claim 1 wherein the patterned metal layer comprises a metal selected from the group consisting of chromium and gold.

10. The method of claim 1 wherein the patterned metal layer comprises a metal ring, and wherein the patterned resist layer does not cover an interior of the ring.

11. The method of claim 1 further comprising the step of removing the patterned resist layer, and then repeating steps (c), (d) and (e).

12. The method of claim 1 wherein the patterned metal layer comprises a metal U-shape.

13. An etched micromechanical apparatus comprising:

a) a semiconductor substrate having an etched pit with semiconductor sidewalls;

b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer has a hole with

dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls

c) a patterned metal layer disposed on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls.

14. The apparatus of claim 13 wherein the patterned metal layer has damaged portions and undamaged portions, and wherein the damaged portions are adjacent to the dielectric sidewalls and semiconductor sidewalls.

15. The apparatus of claim 14 wherein the dielectric layer is unetched in areas adjacent to the undamaged portions of the patterned metal layer.

16. The apparatus of claim 14 wherein the damaged portions of the patterned metal layer are damaged by exposure to an etching process that formed the semiconductor etched pit.

17. The apparatus of claim 13 wherein the semiconductor substrate comprises single crystal silicon and the etched pit is an anisotropically wet etched pit.

18. The apparatus of claim 13 wherein the semiconductor substrate comprises single crystal silicon and the etched pit is a directionally dry etched pit.